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TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

Application Number	09/118,359
Filing Date	July 17, 1998
First Named Inventor	J. Dennis Keller
Art Unit	2823
Examiner Name	Michelle Estrada
Attorney Docket Number	MI22-587

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
- [x] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [x] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please Identify below):

PTO Return Receipt Postcard
$200.00 check
Declaration of Robert C. Hyta
Declaration of Susan M. Schwarz

Remarks

Customer No. 021567

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Wells St. John P.S.		
Signature			
Printed name	Robert C. Hyta		
Date	6/30/06	Reg. No.	46,791

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature	Filed via Express Mail, Receipt No. EV 850820932 US		
Typed or printed name		Date	

EV850820932

PTO/SB/17p (11-05)
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PETITION FEE
Under 37 CFR 1.17(f), (g) & (h)
TRANSMITTAL
(Fees are subject to annual revision)

Send completed form to: Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

Application Number	09/118,359
Filing Date	July 17, 1998
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Enclosed is a petition filed under 37 CFR 1.47(b) **that requires a processing fee (37 CFR 1.17(f), (g), or (h)). Payment of $** 200.00 **is enclosed.**

This form should be included with the above-mentioned petition and faxed or mailed to the Office using the appropriate Mail Stop (e.g., Mail Stop Petition), if applicable. *For transmittal of processing fees under 37 CFR 1.17(i), see form PTO/SB/17i.*

Payment of Fees (small entity amounts are NOT available for the petition fees)

[X] The Commissioner is hereby authorized to charge the following fees to Deposit Account No. 23-0925:
[ ] petition fee under 37 CFR 1.17(f), (g) or (h) [X] any deficiency of fees and credit of any overpayments
Enclose a duplicative copy of this form for fee processing.

[X] Check in the amount of $ 200.00 is enclosed.

[ ] Payment by credit card (Form PTO-2038 or equivalent enclosed). Do not provide credit card information on this form.

Petition Fees under 37 CFR 1.17(f): Fee $400 Fee Code 1462
For petitions filed under:
§ 1.36(a) - for revocation of a power of attorney by fewer than all applicants
§ 1.53(e) - to accord a filing date.
§ 1.57(a) - to accord a filing date.
§ 1.182 - for decision on a question not specifically provided for.
§ 1.183 - to suspend the rules.
§ 1.378(e) - for reconsideration of decision on petition refusing to accept delayed payment of maintenance fee in an expired patent.
§ 1.741(b) - to accord a filing date to an application under § 1.740 for extension of a patent term.

Petition Fees under 37 CFR 1.17(g): Fee $200 Fee Code 1463
For petitions filed under:
§ 1.12 - for access to an assignment record.
§ 1.14 - for access to an application.
§ 1.47 - for filing by other than all the inventors or a person not the inventor.
§ 1.59 - for expungement of information.
§ 1.103(a) - to suspend action in an application.
§ 1.136(b) - for review of a request for extension of time when the provisions of section 1.136(a) are not available.
§ 1.295 - for review of refusal to publish a statutory invention registration.
§ 1.296 - to withdraw a request for publication of a statutory invention registration filed on or after the date the notice of intent to publish issued.
§ 1.377 - for review of decision refusing to accept and record payment of a maintenance fee filed prior to expiration of a patent.
§ 1.550(c) - for patent owner requests for extension of time in ex parte reexamination proceedings.
§ 1.956 - for patent owner requests for extension of time in inter partes reexamination proceedings.
§ 5.12 - for expedited handling of a foreign filing license.
§ 5.15 - for changing the scope of a license.
§ 5.25 - for retroactive license.

Petition Fees under 37 CFR 1.17(h): Fee $130 Fee Code 1464
For petitions filed under:
§ 1.19(g) - to request documents in a form other than that provided in this part.
§ 1.84 - for accepting color drawings or photographs.
§ 1.91 - for entry of a model or exhibit.
§ 1.102(d) - to make an application special.
§ 1.138(c) - to expressly abandon an application to avoid publication.
§ 1.313 - to withdraw an application from issue.
§ 1.314 - to defer issuance of a patent.

Signature	6/30/06 Date
Robert C. Hyta	46,791
Typed or printed name	Registration No., if applicable

EV850820932

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/118,359
Confirmation No. 8927
Filing Date ..... July 17, 1998
Inventor .....J. Dennis Keller et al.
Assignee .....Micron Technology, Inc.
Group Art Unit 2823
Examiner ..... Michelle Estrada
Attorney's Docket No. MI22-587
Customer No. 021567
Title:.....Methods of Forming Floating Gate Transistors

PETITION FOR FILING BY ASSIGNEE

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

From: Robert C. Hyta
Wells St. John P.S.
601 W. First Avenue, Suite 1300
Spokane, WA 99201-3828
Tel. 509-624-4276; Fax 509-838-3424

Applicant Micron Technology, Inc., hereby petitions the Commissioner to accept the filing of the above-identified U.S. Patent Application by Micron Technology, Inc., as the party to which the invention disclosed and claimed in said patent application rightfully belongs, and on behalf of and as agent for Inventors Roger R. Lee and J. Dennis Keller. This Petition and the following listed documents are presented in response to the U.S. Patent and Trademark Office's Notice of Allowability of April 24, 2006, and Objections to oath and declaration contained therein.

United States Patent application Serial No. 09/118,359 was filed on July 17,

1998 with an oath, declaration, and assignment (copies of which are attached). The Examiner objected to the declaration as improper when conveying the notice of allowance. Assignee has attempted to reach Messrs. Lee and Keller to obtain a properly executed oath and declaration to no avail. Assignee hereby petitions under 37 C.F.R. § 1.47(b) to allow Assignee Micron Technology, Inc. to make this application for patent on behalf of and as agent for all inventors to preserve the rights of Micron Technology, Inc.

Referring to the originally filed patent application, Messrs. Lee and Keller transferred all their right, title and interest to the above referenced pending application via a notarized assignment that was recorded in the office of the Assignment Division of the USPTO on July 17, 1998, at Reel/Frame 9341/0748. As evidenced by the accompanying Assignment, Messrs. Lee and Keller have sold, assigned, and transferred the entire right, title and interest in the above-identified application to Micron Technology, Inc., and authorized the Commissioner of Patents and Trademarks to issue such Letters Patent to Micron Technology, Inc., its successors or assigns. Accordingly, Micron Technology, Inc. is entitled to clear title to the subject matter of the application, to the above-identified patent application, and to any patent which issues on the patent application.

Messrs. Lee and Keller are no longer employed by Micron Technology, Inc., and all attempts to have Messrs. Lee and Keller execute a substitute Oath and Declaration have been unsuccessful.

The last known name and address of Mr. Roger R. Lee is as follows:

Roger R. Lee
13501 Crowley Road
Rayville, MO 64084

The last known name and address of Mr. J. Dennis Keller is as follows:

J. Dennis Keller
1840 NW 10041 Avenue
Pembrooke Pines, FL 33028
1(954) 436-6285

Federal Express and Certified Letters as specified below have been sent to both the above addresses enclosing substitute oaths and declarations, and requesting execution of same. The letters sent to Mr. Lee were accepted but no executed declaration has been received. The letters sent to Mr. Keller were returned with an indication that no such person resided at that address. (true copies of the declarations, Federal Express, and Certified Mail labels are submitted herewith). Both internet as well as telephone book searches (aided by directory assistance) have been performed to obtain alternate addresses and/or telephone numbers for Messrs. Lee and Keller. (*see, e.g.*, Declarations of Robert C. Hyta and Susan M. Schwarz (Mr. Hyta's Assistant). Neither Mr. Lee nor Mr. Keller can be found after diligent effort.

The attached Declarations evidence the pertinent facts and the diligent attempts to obtain a substitute Oath or Declaration executed by Messrs. Lee and Keller. The Assignment establishes a chain of title demonstrating Micron Technology, Inc. has ownership in this matter.

As Micron Technology, Inc. has clear title to the above-identified application, and as all attempts to contact Messrs. Lee and Keller to re-execute the Oath and

Declaration have been unsuccessful, Micron Technology, Inc. is believed to be entitled to make such application on behalf and as agent for the inventor pursuant to 37 C.F.R. §1.47(b).

The required fee pursuant to 37 C.F.R. §1.17(g) is enclosed.

The accompanying documents and payment satisfy the requirements of 37 C.F.R. §1.47(b) for filing when an inventor cannot be found or reached after diligent effort. Applicant therefore requests that the petition be granted. Further, the filing and granting of this petition, together with the enclosed payment, satisfies the Patent and Trademark Office's (PTO) requirement regarding the oath and declaration. Applicant therefore requests that the PTO provide formal notification that the objection to oath and declaration has been withdrawn.

The Examiner is requested to telephone the undersigned if the Examiner believes such would facilitate prosecution of the present application. The undersigned is available for telephone consultation at any time during normal business hours (Pacific Standard Time).

Respectfully submitted,

Dated: 6/30/06 By: _____

Robert C. Hyta
Reg. No. 46,791

- END OF DOCUMENT -

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

Methods Of Enhancing Data Retention Of A Floating Gate Transistor, Methods Of Forming Floating Gate Transistors, And Floating Gate Transistors

* * * * *

INVENTORS

J. Dennis Keller
Roger R. Lee

ATTORNEY'S DOCKET NO. MI22-587

TECHNICAL FIELD

This invention relates to floating gate transistors and methods of forming the same. This invention also relates to methods of enhancing data retention of floating gate transistors.

BACKGROUND OF THE INVENTION

Floating gate transistors are utilized in some semiconductor memory cells. One type of memory cell that uses a floating gate transistor is a flash erasable and programmable read only memory (EPROM). A floating gate transistor typically includes a tunnel dielectric layer, a floating gate, an interlayer dielectric and a control gate or word line. Source/drain regions are formed operatively adjacent the floating gate and within semiconductive substrate material. A floating gate transistor can be placed in a programmed state by storing charge on the floating gate of the floating gate transistor. Typically, a large voltage, e.g. 25 volts, between the control gate and the substrate allow some electrons to cross the interlayer dielectric and charge the floating gate. The "data retention" of a floating gate transistor refers to the ability of the transistor to retain its charge over a period of time. Charge can be lost, undesirably, through electron migration from the floating gate through various adjacent materials. One problem which has confronted the industry is electron migration through the interlayer dielectric material immediately above the floating gate. The thickness of the interlayer dielectric material has an impact

on the ability of a floating gate to retain its charge. Thinner regions of the interlayer dielectric material provide undesired migration paths for electrons to leave the programmed floating gate relative to other thicker regions of the interlayer dielectric material. Hence, non-uniformity in the thickness of the interlayer dielectric material is undesirable.

A contributing factor to a non-uniformly thick interlayer dielectric material is the presence of a large number of grain boundaries at the interlayer dielectric/floating gate interface. Conductive doping of the floating gate, as is desirable, undesirably increases the number of interface grain boundaries, which in turn, increases the chances of having a non-uniformly thick interlayer dielectric.

This invention grew out of concerns associated with improving the data retention characteristics of floating gate transistors.

SUMMARY OF THE INVENTION

Floating gate transistors and methods of forming the same are described. In one implementation, a floating gate is formed over a substrate. The floating gate has an inner first portion and an outer second portion. Conductivity enhancing impurity is provided in the inner first portion to a greater concentration than conductivity enhancing impurity in the outer second portion. In another implementation, the floating gate is formed from a first layer of conductively doped semiconductive material and a second layer of substantially undoped semiconductive material. In another implementation, the floating gate

is formed from a first material having a first average grain size and a second material having a second average grain size which is larger than the first average grain size.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment at one processing step in accordance with the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 4.

Fig. 6 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 5.

Fig. 7 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 6.

Fig. 8 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 7.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, a fragmentary portion of a semiconductor wafer is shown generally at 10 and comprises a semiconductive substrate 12. As used in this document, the term "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Referring to Fig. 2, a layer 14 is formed over substrate 12 and constitutes a tunnel oxide layer.

Referring to Fig 3, a layer 16 is formed over substrate 12. In a preferred implementation, layer 16 constitutes a polysilicon layer which is formed to a first thickness t_1. Preferably, the polysilicon of layer 16 is undoped as formed and is subsequently doped, as through ion implantation, with conductivity enhancing impurity to a desired degree. According to one aspect, layer 16 is doped with a suitable impurity which is sufficient to define a sheet resistance of between 300 ohm/sq. and 400 ohm/sq. According to another aspect, first layer 16 is doped

with an impurity concentration which is greater than or equal to about 1 x $10^{18}cm^{-3}$. An exemplary concentration is between about 1 x $10^{18}cm^{-3}$ and 1 x $10^{20}cm^{-3}$, or greater. A suitable and preferred dopant or impurity is phosphorous. When phosphorous is utilized, the preferred sheet resistance is between about 600 ohm/sq. and 700 ohm/sq.

Alternately considered, layer 16 constitutes a first material or silicon-containing volume which is formed over the substrate and doped with a suitable impurity concentration to define a first average grain size. Accordingly, such silicon-containing volume has a first average grain boundary area per unit volume. An exemplary grain size is between about 50-100 nm, or about 10-25 grain boundaries in an erase area of 0.2 μm^2 to 0.4 μm^2.

Referring to Fig. 4, a second layer 18 is formed over the substrate 12 and first layer 16. Preferably, layer 18 is formed directly atop layer 16 and to a second thickness t_2. Preferably, second layer 18 constitutes a material such as polysilicon or amorphous silicon which is substantially undoped relative to first layer 16. The term "substantially undoped" as used within this document will be understood to mean having an impurity concentration which is less than 1 x $10^{18}cm^{-3}$. In accordance with one aspect of the invention, second layer 18 constitutes a second material which is formed over material of layer 16 to have a second average grain size which is larger than the first average grain size of layer 16. Accordingly, second layer 18 constitutes a second

silicon-containing volume having a second grain boundary area per unit volume which is less than the first grain boundary area per unit volume. An exemplary grain size is between about 100-200 nm, or greater than about 25 grain boundaries in an erase area of 0.2 μm^2 to 0.4 μm^2.

In a preferred implementation, the material of layers 16, 18, taken together, constitute material from which a floating gate of a floating gate transistor will be formed. Layers 16, 18 define an aggregate or combined thickness ($t_1 + t_2$). Accordingly to one aspect, the combined thickness of layers 16, 18 is less than or equal to about 1000 Angstroms. Such combined thickness can, however, range upward to around 1500 Angstroms or greater. The combined thickness can range downward as well. This is especially true as advances in scalability result in smaller floating gate dimensions. In one implementation, the first and second thicknesses are substantially the same. Accordingly, when the aggregate or combined thickness is around 1000 Angstroms, individual thicknesses t_1 and t_2 would be around 500 Angstroms. In another implementation, first and second thicknesses t_1 and t_2 can be different from one another. Accordingly, first thickness t_1 can constitute less than or equal to about 75% of the aggregate thickness. In another implementation, first thickness t_1 can constitute at least 25% of the aggregate or combined thickness of the floating gate. In yet another implementation, layer 16 can comprise between about 25-75% of the floating gate thickness. Where the aggregate thickness is

about 1000 Angstroms, the first thickness would be between 250-750 Angstroms. First thickness t_1 can be less than 550 Angstroms, or between 450 Angstroms and 550 Angstroms. In another implementation, the combined or aggregate thickness ($t_1 + t_2$) can equal around about 500 Angstroms, with thickness t_1 being equal to around 25-50 Angstroms. Other relative thickness relationships are of course possible.

Referring still to Fig. 4, layers 16 and 18 are subjected to suitable floating gate definition steps. In a first step, floating gate material 16, 18 is etched into and out of the plane of the page upon which Fig. 4 appears. Such effectively defines so-called floating gate wings which overlie field oxide which is not specifically shown in the Fig. 4 construction. The first etch partially forms a plurality of floating gates having respective inner first portions (layer 16) disposed proximate the substrate, and respective outer second portions (layer 18) disposed over the first portions.

Referring to Fig. 5, substrate 12 is subjected to suitable oxidizing conditions which are effective to form a first oxide layer 20 over second layer 18. Layer 20 constitutes a bottom oxide layer which is formed to a thickness of between about 50 Angstroms to 100 Angstroms.

Referring to Fig. 6, a layer 22 is formed over substrate 12 and preferably constitutes a nitride layer which is formed over first oxide layer 20. Substrate 12 is subsequently subjected to oxidizing conditions which are sufficient to form a second oxide layer 24 over nitride layer 22. Taken together, layers 20, 22, and 24 constitute an ONO

dielectric layer which constitutes a third layer 26 of dielectric material which is formed over the second silicon-containing volume or second layer 18. Other dielectric layers are possible.

Referring to Fig. 7, a fourth layer 28 is formed over third layer 26 and comprises a conductive material. In a preferred implementation, layer 28 constitutes a third layer of polysilicon which is formed over second oxide layer 24 and will constitute a conductive line for the floating gate transistor to be formed.

Referring to Fig. 8, the various layers of Fig. 7 are etched to provide a plurality of floating gate transistors 30, 32, 34, and 36. Such defines the remaining opposing edges of the floating gates of such transistors. The floating gate transistors are also provided with respective source/drain regions which are disposed laterally proximate the floating gates. In the illustrated example, individual source regions 38, 40 and a drain region 42 are shown. Additionally, an oxide layer 44 is disposed over individual floating gates 30, 32, 34, and 36. A plug 46 comprising conductive contact film material is disposed operatively adjacent drain region 42 and serves to electrically connect with such drain region. A barrier layer 48, metal layer 50 and a passivation layer 52 are shown.

The above-described floating gate construction provides an improved floating gate transistor which is less prone to lose its charge due to electron migration from the floating gate through the dielectric layer intermediate the floating gate and the overlying word line. Such

improvements increase the data retention characteristics of the floating gate. The improvements are made possible, in part, through a more uniformly thick bottom oxide layer (oxide layer 20) of the ONO dielectric layer discussed above. Such a uniformly thick layer provides less opportunities for electrons to migrate away from the floating gate.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS:

1. A method for enhancing data retention of a floating gate transistor comprising:

forming a floating gate over a substrate, the floating gate having an inner first portion and an outer second portion; and

providing conductivity enhancing impurity in the inner first portion to a greater concentration than conductivity enhancing impurity in the outer second portion.

2. The method of claim 1, wherein the forming of the floating gate comprises forming the inner first portion and the outer second portion to comprise polysilicon.

3. The method of claim 1, wherein the floating gate has a thickness, and the forming of the floating gate comprises forming the inner first portion to comprise at least 25 percent of the floating gate thickness.

4. The method of claim 1, wherein the floating gate has a thickness, and the forming of the floating gate comprises forming the inner first portion to comprise between about 25 to 75 percent of the floating gate thickness.

5. The method of claim 1, wherein the providing of conductivity enhancing impurity in the inner first portion comprises doping the inner first portion to a dopant concentration greater than or equal to 1 x $10^{18}cm^{-3}$.

6. The method of claim 1, wherein the providing of conductivity enhancing impurity in the inner first portion comprises doping the inner first portion to a dopant concentration of greater than or equal to about 1 x $10^{18}cm^{-3}$, with the outer second portion having a dopant concentration of less than 1 x $10^{18}cm^{-3}$.

7. The method of claim 1, wherein:

the forming of the floating gate comprises forming a first layer of polysilicon over the substrate, the first layer defining the inner first portion, and after the forming of the first layer forming a second layer of polysilicon, the second layer defining the outer second portion.

8. The method of claim 1, wherein:

the forming of the floating gate comprises forming a first layer of polysilicon over the substrate, the first layer defining the inner first portion, and after the forming of the first layer forming a second layer of polysilicon, the second layer defining the outer second portion; and

intermediate the forming of the first and second layers, providing the conductivity enhancing impurity in the inner first portion to a dopant concentration of greater than or equal to about $1 \times 10^{18} cm^{-3}$.

9. A method of forming a floating gate transistor comprising:

forming a first layer of conductively doped semiconductive material over a semiconductive substrate;

forming a second layer of substantially undoped semiconductive material over the first layer;

forming a third layer comprising dielectric material over the second layer;

forming a fourth layer comprising conductive material over the third layer; and

forming a floating gate transistor comprising the first, second, third, and fourth layers.

10. The method of claim 9, wherein the first and second layers comprise a floating gate having a thickness, and the forming of the first and second layers comprise forming the first layer to occupy at least 25 percent of the floating gate thickness.

11. The method of claim 9, wherein the first and second layers comprise a floating gate having a thickness, and the forming of the first and second layers comprise forming the first layer to occupy less than 75 percent of the floating gate thickness.

12. The method of claim 9, wherein the forming of the first layer comprises forming the first layer to have a dopant concentration of greater than or equal to about $1 \times 10^{18} cm^{-3}$.

13. The method of claim 9, wherein the forming of the first layer comprises:

forming a layer of polysilicon over the substrate; and

doping the polysilicon layer with phosphorous dopant material to a concentration of greater than or equal to about $1 \times 10^{18} cm^{-3}$.

14. The method of claim 9, wherein:

the first and second layers comprise a floating gate having a thickness, and the forming of the first and second layers comprise forming the first layer to occupy less than 75 percent of the floating gate thickness; and

the forming of the first layer comprises forming the first layer to have a dopant concentration of greater than or equal to about $1 \times 10^{18} cm^{-3}$.

15. A method of forming a floating gate comprising:

forming a first material over a substrate, the first material having a first average grain size;

forming a second material over the first material, the second material having a second average grain size, the second average grain size being larger than the first average grain size; and

providing the first and second materials into a desired floating gate shape.

16. The method of claim 15, wherein the forming of the first material comprises forming conductively doped polysilicon to have a sheet resistance of between 300 ohm/sq. and 400 ohm/sq..

17. The method of claim 15, wherein:

the forming of the first material comprises forming conductively doped polysilicon to have a sheet resistance of between 300 ohm/sq. and 400 ohm/sq.; and

the forming of the second material comprises forming polysilicon to have a sheet resistance greater than 400 ohm/sq..

18. The method of claim 15, wherein the forming of the first material comprises forming conductively doped polysilicon to have a dopant concentration greater than or equal to about $1 \times 10^{18} cm^{-3}$.

19. The method of claim 15, wherein the forming of the second material comprises forming the second material directly atop the first material.

20. The method of claim 15, wherein the forming of the second material comprises forming the second material directly atop the first material, the first and second materials having a combined thickness of less than or equal to about 1000 Angstroms, the first material having an individual thickness of less than about 75 percent of the combined thickness.

21. A method of forming a floating gate transistor comprising:

forming a floating gate over a substrate, the floating gate comprising a first silicon-containing volume having a first grain boundary area per unit volume, and a second silicon-containing volume over the first silicon-containing volume having a second grain boundary area per unit volume, the second grain boundary area per unit volume being less than the first grain boundary area per unit volume;

forming a dielectric layer over the second silicon-containing volume; and

forming a conductive line over the dielectric layer to provide a floating gate transistor.

22. The method of claim 21, wherein the forming of the dielectric layer comprises forming an oxide layer atop the second silicon-containing volume.

23. The method of claim 21, wherein the forming of the floating gate comprises:

forming a first layer of conductively doped polysilicon over the substrate, the first layer constituting the first silicon-containing volume and having a dopant concentration of greater than or equal to about 1 x $10^{18}cm^{-3}$ and a sheet resistance of between about 300 ohm/sq. and 400 ohm/sq..

24. The method of claim 21, wherein the forming of the floating gate comprises:

forming a first layer of conductively doped polysilicon over the substrate, the first layer constituting the first silicon-containing volume and having a dopant concentration of greater than or equal to about 1 x $10^{18}cm^{-3}$ and a sheet resistance of between about 300 ohm/sq. and 400 ohm/sq.; and

after forming the first layer, forming a second layer of polysilicon over the first layer, the second layer constituting the second silicon-containing volume and having a dopant concentration less than about 1 x $10^{18}cm^{-3}$ and a sheet resistant greater than 400 ohm/sq..

25. A method of forming a floating gate transistor comprising:

forming a first layer of polysilicon over a substrate to a first thickness;

doping the first layer to a degree sufficient to define a sheet resistance of between 300 ohm/sq. and 400 ohm/sq.;

after the doping, forming a second layer of polysilicon over the first layer of polysilicon to a second thickness;

oxidizing the substrate to form a first oxide layer over the second layer of polysilicon;

forming a layer of nitride over the first oxide layer;

oxidizing the substrate to form a second oxide layer over the layer of nitride;

forming a third layer of polysilicon over the second oxide layer; and

etching at least some of the layers to provide a floating gate transistor over the substrate.

26. The method of claim 25, wherein the first and second thicknesses are substantially the same.

27. The method of claim 25, wherein the first and second thicknesses are different.

28. The method of claim 25, wherein the first and second thicknesses comprise an aggregate thickness and the first thickness constitutes less than or equal to about 75 percent of the aggregate thickness.

29. The method of claim 25, wherein the first thickness is less than about 550 Angstroms.

30. The method of claim 25, wherein the first thickness is between 450 Angstroms and 550 Angstroms.

31. The method of claim 25, wherein the forming of the second layer of polysilicon comprises forming the layer to have a sheet resistance which is greater than the sheet resistance of the first layer of polysilicon.

32. A floating gate transistor comprising:

a substrate; and

a floating gate over the substrate having an inner first portion and an outer second portion, the inner first portion being disposed proximate the substrate and the outer second portion being disposed over the inner first portion, the inner first portion containing a concentration of conductivity enhancing impurity which is greater than a concentration of conductivity enhancing impurity contained by the outer second portion;

a dielectric layer disposed over the outer second portion;

a conductive line disposed over the dielectric layer; and

source/drain regions laterally proximate the floating gate.

33. The floating gate transistor of claim 32, wherein the inner first portion contains an impurity concentration of greater than or equal to about $1 \times 10^{18}cm^{-3}$.

34. The floating gate transistor of claim 32, wherein the inner first portion contains an impurity concentration of greater than or equal to about $1 \times 10^{18}cm^{-3}$, and the outer second portion contains an impurity concentration of less than $1 \times 10^{18}cm^{-3}$.

35. The floating gate transistor of claim 32, wherein the floating gate has a thickness, and the inner first portion constitutes less than about 75 percent of the floating gate thickness.

36. The floating gate transistor of claim 32, wherein the floating gate has a thickness, and the inner first portion constitutes less than or equal to about 50 percent of the floating gate thickness.

37. A floating gate transistor comprising:

a substrate;

a floating gate over the substrate comprising a first material having a first average grain size and a second material disposed over the first material and having a second average grain size which is larger than the first average grain size;

a dielectric layer disposed over the second material;

a conductive line disposed over the dielectric layer; and

source/drain regions laterally proximate the floating gate.

38. The floating gate transistor of claim 37, wherein the first material has a sheet resistance of less than about 400 ohm/sq..

39. The floating gate transistor of claim 37, wherein the first and second materials define an aggregate thickness and the first material occupies less than 75 percent of the aggregate thickness.

40. The floating gate transistor of claim 37, wherein the first and second material have individual respective thicknesses and the first material thickness is less than the second material thickness.

ABSTRACT OF THE DISCLOSURE

Floating gate transistors and methods of forming the same are described. In one implementation, a floating gate is formed over a substrate. The floating gate has an inner first portion and an outer second portion. Conductivity enhancing impurity is provided in the inner first portion to a greater concentration than conductivity enhancing impurity in the outer second portion. In another implementation, the floating gate is formed from a first layer of conductively doped semiconductive material and a second layer of substantially undoped semiconductive material. In another implementation, the floating gate is formed from a first material having a first average grain size and a second material having a second average grain size which is larger than the first average grain size.

DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: Methods of Enhancing Data Retention of a Floating Gate Transistor, Methods of Forming Floating Gate Transistors, and Floating Gate Transistors, the specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful

false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * * * * * * * *

Full name of inventor: **J. Dennis Keller**

Inventor's Signature: J. Dennis Keller

Date: 7/1/98

Residence: **Boise, Idaho**

Citizenship: **U.S.A.**

Post Office Address: **1863 S. Londoner Way**
Boise, ID 83706

* * * * * * * * * * *

Full name of inventor: **Roger R. Lee**

Inventor's Signature: Roger R. Lee

Date: 7-1-98

Residence: **Boise, Idaho**

Citizenship: **U.S.A.**

Post Office Address: ~~**335 Raindrop**~~ 3936 N. BURNSTEAD
Boise, ID 83706 BOISE ID 83704

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OCTOBER 14, 1998

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WELLS, ST. JOHN ET AL
LANCE R. SADLER
601 W. FIRST AVENUE, SUITE 1300
SPOKANE, WASHINGTON 99201-3817

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RECORDATION DATE: 07/17/1998

REEL/FRAME: 9341/0748
NUMBER OF PAGES: 5

BRIEF: ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS).

ASSIGNOR:
KELLER, J. DENNIS

DOC DATE: 07/01/1998

ASSIGNOR:
LEE, ROGER R.

DOC DATE: 07/01/1998

ASSIGNEE:
MICRON TECHNOLOGY, INC.
8000 SOUTH FEDERAL WAY
BOISE, IDAHO 83706

SERIAL NUMBER: 09118359
PATENT NUMBER:

FILING DATE: 07/17/1998
ISSUE DATE:

STEVEN POST, EXAMINER
ASSIGNMENT DIVISION
OFFICE OF PUBLIC RECORDS

ASSIGNMENT

PARTIES TO THE ASSIGNMENT:

INVENTORS:

J. Dennis Keller

Roger R. Lee

ASSIGNEE:

Micron Technology, Inc.
Corporation of the State of Delaware
8000 South Federal Way
Boise, Idaho 83706-9632

BACKGROUND OF THIS ASSIGNMENT:

INVENTORS have conceived certain new and useful inventions disclosed in a United States patent application titled Methods of Enhancing Data Retention of a Floating Gate Transistor, Methods of Forming Floating Gate Transistors, and Floating Gate Transistors.

MICRON TECHNOLOGY, INC. desires to acquire the entire right, title and interest in said inventions and with respect to any Letters Patent that may be granted with respect to the inventions in both the United States and in all foreign countries.

THE PARTIES AGREE AS FOLLOWS:

In consideration of good and valuable consideration, the receipt sufficiency and adequacy of which is hereby acknowledged, INVENTORS hereby sell, assign and transfer to MICRON TECHNOLOGY, INC. the entire right, title and interest in the above-identified application executed

currently with this assignment and to any reissues, renewals, divisions or continuations thereof, and hereby authorizes the Commissioner of Patents and Trademarks to issue such Letters Patent to MICRON TECHNOLOGY, INC., for the sole use of MICRON TECHNOLOGY, INC., its successors or assigns.

INVENTORS further agree to execute, at the request and expense of MICRON TECHNOLOGY, INC. such other formal documents as may be required to fully convey the interest transferred herein and will similarly execute any application papers required for the filing of any division, continuation, renewal or reissue of the patent application or resulting Letters Patent; and will generally do everything necessary or desirable to obtain and enforce proper protection for the inventions assigned hereby.

INVENTORS further assign to MICRON TECHNOLOGY, INC. the whole right, title and interest in the inventions disclosed in the application throughout all countries foreign to the United States. MICRON TECHNOLOGY, INC. is hereby authorized to apply for patents relating to the inventions in its own name in countries where such procedure is proper; to claim the benefit of the International Convention; to file and prosecute International Applications relating to the inventions under the Patent Cooperation Treaty; and to file and prosecute applications relating to the inventions under the European Patent Convention. INVENTORS agree to execute applications relating to the inventions in those countries and under those conventions where

it is necessary that the same be executed by the inventor, and to execute assignments of such applications and the resulting Letters Patent to MICRON TECHNOLOGY, INC. as well as all other necessary papers in relation to such applications and Letters Patent.

INVENTORS further warrant and covenant that no assignment, grant, mortgage, license or other agreement affecting the rights and property herein conveyed has been or will be made to others by the undersigned, and that the full rights to convey the same as herein expressed is possessed by the undersigned.

To be binding on the heirs, assigns, representatives and successors of the undersigned and extend to the successors, assigns and nominees of the Assignees.

(Signature) J. Dennis Keller Date: 7/1/98

J. Dennis Keller

State of Idaho)
) ss.
County of Ada)

BEFORE ME, this 1st day of July 1998 personally appeared the above-named inventor, to me known to be the person who is described in and who executed the foregoing assignment instrument and acknowledged to me that he/she executed the same of his/her own free will for the purpose therein expressed.

SEAL LORI MURPHY NOTARY PUBLIC STATE OF IDAHO

Lori Murphy
Notary or Consular Officer
My Commission Expires: 6-12-2002

(Signature) _____ Date: 7-15-98
Roger R. Lee

State of Idaho)
) ss.
County of Ada)

BEFORE ME, this 15th day of July 1998 personally appeared the above-named inventor, to me known to be the person who is described in and who executed the foregoing assignment instrument and acknowledged to me that he/she executed the same of his/her own free will for the purpose therein expressed.

SEAL

NOTARY PUBLIC STATE OF IDAHO

_____
Notary or Consular Officer
My Commission Expires: 6-12-2002

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07-30-1998

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1. Name of Conveying Part(ies):

J. Dennis Keller
Roger R. Lee

Additional name(s) of conveying party(ies) attached? ☐ Yes ☑ No

2. Name and address of receiving party(ies):

Name: Micron Technology, Inc.

Internal Address:

Street Address: 8000 South Federal Way

City: Boise State: ID Zip: 83706

Additional names(s) & address(es) attached: ☐ Yes ☑ No

3. Nature of conveyance:

☑ Assignment ☐ Security Agreement
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☐ Other

Execution Date: 07/01/98

4. Application number(s) or patent number(s):
If this document is being filed together with a new application, the execution date of the application is: 07/01/98

09-118359

A. Patent Application No.(s):

40.00 DP

B. Patent No.(s)

Additional numbers attached: ☐ Yes ☑ No

Additional numbers attached: ☐ Yes ☑ No

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: Lance R. Sadler

Internal Address: Wells, St. John, Roberts, Gregory & Matkin P.S.

Street Address: 601 W. First Avenue, Ste. 1300

City: Spokane State: WA Zip: 99201-3817

6. Total number of applications and patents involved. 1

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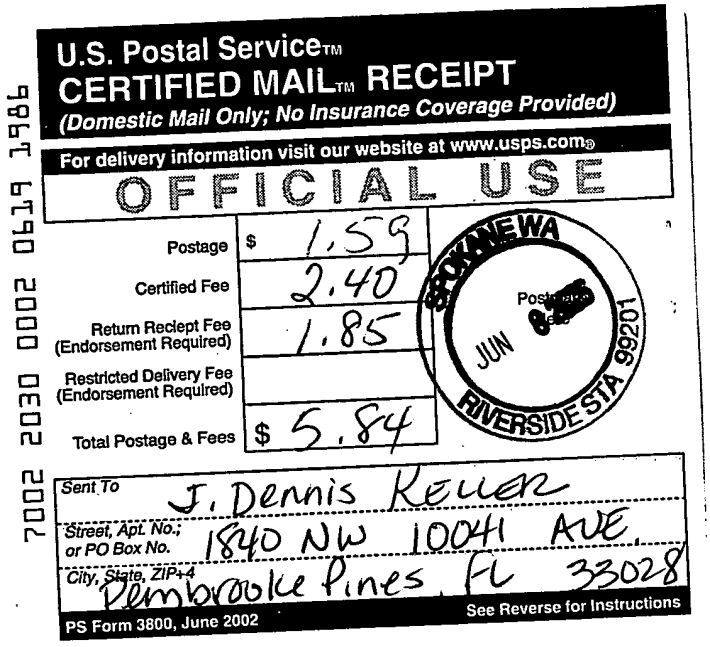

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As the below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and joint inventor with Roger R. Lee of the subject matter which is claimed and for which a patent is sought on the invention entitled: Methods of Enhancing Data Retention of a Floating Gate Transistor, Methods of Forming Floating Gate Transistors, and Floating Gate Transistors, the specification of which is attached hereto.

On behalf of myself and Roger R. Lee, I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

On behalf of myself and Roger R. Lee, I acknowledge the duty to disclose information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations §1.56.

PRIOR FOREIGN APPLICATIONS:

On behalf of myself and Roger R. Lee, I hereby state that no applications for foreign patents or inventor's certificates have been filed prior to the date of execution of this declaration.

On behalf of myself and Roger R. Lee, I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that

such willful false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * * * * * * *

Full name of inventor: **J. Dennis Keller**

Inventor's Signature: _____

Date: _____

Residence: **Pembrooke Pines, Florida**

Citizenship: **U.S.A.**

Post Office Address: **1840 NW 10041 Ave.**
Pembrooke Pines, FL 33028

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DECLARATION OF JOINT INVENTORS FOR PATENT APPLICATION

As the below named inventor, I hereby declare that:

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I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

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PRIOR FOREIGN APPLICATIONS:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful

false statement may jeopardize the validity of the application or any patent issued therefrom.

* * * * * * * * * *

Full name of inventor: **J. Dennis Keller**

Inventor's Signature: _____

Date: _____

Residence: **Boise, Idaho**

Citizenship: **U.S.A.**

Post Office Address: **1863 S. Londoner Way**
Boise, ID 83706

* * * * * * * * * *

Full name of inventor: **Roger R. Lee**

Inventor's Signature: _____

Date: _____

Residence: **Rayville, Missouri**

Citizenship: **U.S.A.**

Post Office Address: **13501 Crowley Road**
Rayville, MO 64084

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/118,359
Confirmation No. 8927
Filing Date ..... July 17, 1998
Inventor .....J. Dennis Keller et al.
Assignee .....Micron Technology, Inc.
Group Art Unit 2823
Examiner ..... Michelle Estrada
Attorney's Docket No. MI22-587
Customer No. 021567
Title:.....Methods of Forming Floating Gate Transistors

DECLARATION OF ROBERT C. HYTA

I, Robert C. Hyta, am an attorney licensed to practice before the USPTO and in Indiana and Washington, and represent Micron Technology, Inc., in matters relating to patent prosecution.

Micron Technology, Inc., was contacted to obtain the last known addresses of former employees J. Dennis Keller and Roger R. Lee.

As specified below, I executed letters enclosing oath and declarations to J. Dennis Keller and Roger R. Lee at the respective addresses below via Federal Express and Certified Mail.

A first letter (a copy of which is attached), addressed to Roger R. Lee, requesting he contact our office regarding the above referenced application was mailed via Certified Mail, Return Receipt Requested, on January 24, 2006, to his last known address at 13501 Crowley Road, Rayville, MO 64084. Our records indicate the letter was received and signed for by Tami S. Lee on January 31, 2006.

A second letter (a copy of which is attached) enclosing copies of the Application

for Letters Patent and Declaration of Joint Inventors as filed with the USPTO on July 17, 1998, and enclosing a revised Declaration for signature as well as a pre-paid Federal Express envelope, was sent to Inventor Roger R. Lee at his last known address via Federal Express on February 9, 2006. The second letter explained the original Declaration had been objected to by the Patent Examiner due to the alteration of Mr. Lee's Post Office Address at the time of signature without his initials. Our records indicate the Federal Express package was delivered on February 10, 2006. To my knowledge, Wells St. John has not received the signed revised Declaration from Mr. Lee.

I conducted internet searches for Roger R. Lee using Google and Yahoo search engines. I also conducted a phone book search utilizing directory assistance. No alternative addresses or a phone number for Roger R. Lee were obtained.

A third letter (copy of which is attached hereto) enclosing copies of the Application for Letters Patent and Declaration of Joint Inventors as filed with the USPTO on July 17, 1998, and enclosing a revised Declaration for signature by Joint Inventor J. Dennis Keller on behalf of Inventor Roger R. Lee was sent to Inventor J. Dennis Keller at his last known address of 1840 NW 10041 Avenue, Pembrooke Pines, FL 33028, via both Federal Express and Certified Mail, Return Receipt Requested, on June 8, 2006. Our records indicate the Federal Express package was delivered to the address on June 9. The original Certified Mail package mailed June 8, 2006 was returned to our office on June 27, 2006, undelivered, forwarding order expired.

I conducted internet searches for J. Dennis Keller using Google and Yahoo search engines. I also conducted a phone book search utilizing directory assistance. No alternative addresses for J. Dennis Keller were obtained.

Dated: 6/30/06

Robert C. Hyta

Wells St. John
PROFESSIONAL SERVICE

PATENTS ■ TRADEMARKS ■ COPYRIGHTS

601 W. 1st Avenue, Suite 1300
Spokane, WA 99201-3828
(509) 624-4276
FAX (509) 838-3424
www.wellsstjohn.com

January 24, 2006

CERTIFIED MAIL
Return Receipt Requested

Mr. Roger R. Lee
13501 Crowley Road
Rayville, MO 64084

Re: U.S.A. Patent Application Serial No. 09/118,359
"Methods of Forming Floating Gate Transistors"
Our File No.: MI22-587

Dear Mr. Lee:

Please contact me at your earliest convenience at (509) 624-4276 regarding the above-referenced Micron Patent Application.

Regards,

Robert C. Hyta

RCH/sms
cc: Art Tyczka

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February 9, 2006

Via Federal Express

Mr. Roger R. Lee
13501 Crowley Road
Rayville, MO 64084

Re: U.S.A. Patent Application Serial No. 09/118,359
"Methods of Forming Floating Gate Transistors"
Our File No.: MI22-587
Micron File No.: 96-0574.00/US

Dear Mr. Lee:

Enclosed please find copy of the above-referenced Application for Letters Patent and Declaration of Joint Inventors as filed with the USPTO on July 17, 1998.

The original Declaration as signed by you has been objected to by the Patent Examiner due to the alteration of your Post Office Address at the time of signature without your initials.

Therefore, enclosed please find revised Declaration of Joint Inventors with your current address. Please sign and date where indicated on Page 2 thereof, and return the Declaration to my office in the enclosed prepaid Federal Express envelope.

Thank you in advance for your cooperation with respect to this matter, and should you have any questions or concerns, please do not hesitate to contact me immediately.

Sincerely,

Robert C. Hyta

RCH/sms
Enclosures: As referenced above
cc: Art Tyczka

S:\MI22\587\035.doc

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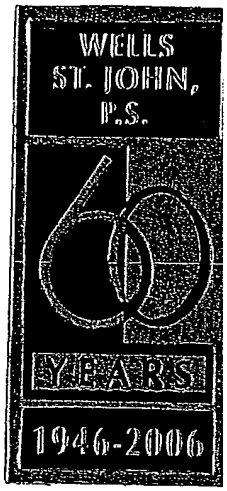

June 8, 2006

Via Federal Express and Certified Mail

Mr. J. Dennis Keller
1840 NW 10041 Ave
Pembrooke Pines, FL 33028

Re: U.S.A. Patent Application Serial No. 09/118,359
"Methods of Forming Floating Gate Transistors"
Our File No.: MI22-587
Micron File No.: 96-0574.00/US

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The original Declaration as signed by Mr. Lee has been objected to by the Patent Examiner due to the alteration of his Post Office Address at the time of signature without his initials. We have attempted to reach Mr. Lee, but have been unable to do so.

To facilitate issuance of this application, enclosed please find a revised Declaration of Joint Inventors made by you recognizing the inventorship of Mr. Lee. Please sign and date where indicated, and return the Declaration to my office in the enclosed prepaid Federal Express envelope. If you wish to revise the declaration, please initial and date next to all revisions.

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Thank you in advance for your cooperation with respect to this matter, and should you have any questions or concerns, please do not hesitate to contact me immediately.

Sincerely,

Robert C. Hyta

RCH/sms
Enclosures: As referenced above
cc: Art Tyczka

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/118,359
Confirmation No. 8927
Filing Date ..... July 17, 1998
Inventor .....J. Dennis Keller et al.
Assignee .....Micron Technology, Inc.
Group Art Unit 2823
Examiner ..... Michelle Estrada
Attorney's Docket No. MI22-587
Customer No. 021567
Title: .....Methods of Forming Floating Gate Transistors

DECLARATION OF SUSAN M. SCHWARZ

I, Susan M. Schwarz, am employed as a legal assistant at the law firm of Wells St. John, P.S and more specifically as assistant to Attorney Robert C. Hyta

Upon instruction from Mr. Hyta I prepared and forwarded cover letters and oath and declarations to J. Dennis Keller and Roger R. Lee at the respective addresses below as specified below via Federal Express and Certified Mail.

Our records indicate a letter (a copy of which is attached) addressed to Roger R. Lee requesting he contact our office regarding the above referenced application was mailed via Certified Mail, Return Receipt Requested, on January 24, 2006, to his last known address at 13501 Crowley Road, Rayville, MO 64084. Our records indicate the letter was received and signed for by Tami S. Lee on January 31, 2006.

Our records indicate a letter (a copy of which is attached) enclosing copies of the Application for Letters Patent and Declaration of Joint Inventors as filed with the USPTO on July 17, 1998, and enclosing a revised Declaration for signature as well as a pre-paid Federal Express envelope was sent to Inventor Roger R. Lee to his last known

address via Federal Express on February 9, 2006. The letter explained the original Declaration had been objected to by the Patent Examiner due to the alteration of Mr. Lee's Post Office Address at the time of signature without his initials. Our records indicate the Federal Express package was delivered on February 10, 2006. To my knowledge, Wells St. John has not received the signed revised Declaration from Mr. Lee.

Another letter (copy of which is attached hereto) enclosing copies of the Application for Letters Patent and Declaration of Joint Inventors as filed with the USPTO on July 17, 1998, and enclosing a revised Declaration for signature by Joint Inventor J. Dennis Keller on behalf of Inventor Roger R. Lee was sent to Inventor J. Dennis Keller to his last known address at 1840 NW 10041 Avenue, Pembrooke Pines, FL 33028, via both Federal Express and Certified Mail, Return Receipt Requested, on June 8, 2006. Our records indicate the Federal Express package was delivered to the address on June 9.

On June 9, 2006, I was contacted by the current homeowner of the residence located at 1840 NW 10041 Avenue, Pembrooke Pines, Florida, a Ms. Denise Angeloni. Ms. Angeloni retrieved our Federal Express envelope from her front porch and advised she purchased the residence over two years ago from a relative of J. Dennis Keller. Ms. Angeloni was unable to provide a forwarding address or telephone number for either Mr. Keller or the former owner of the residence.

The original Certified Mail package mailed June 8, 2006 was returned to our office on June 27, 2006, undelivered, forwarding order expired.

Dated: 6/30/06

Susan M. Schwarz

Wells St.John
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601 W. 1st Avenue, Suite 1300
Spokane, WA 99201-3828
(509) 624-4276
FAX (509) 838-3424
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January 24, 2006

CERTIFIED MAIL
Return Receipt Requested

Mr. Roger R. Lee
13501 Crowley Road
Rayville, MO 64084

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"Methods of Forming Floating Gate Transistors"
Our File No.: MI22-587

Dear Mr. Lee:

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Regards,

Robert C. Hyta

RCH/sms
cc: Art Tyczka

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February 9, 2006

Via Federal Express

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Thank you in advance for your cooperation with respect to this matter, and should you have any questions or concerns, please do not hesitate to contact me immediately.

Sincerely,

Robert C. Hyta

RCH/sms
Enclosures: As referenced above
cc: Art Tyczka

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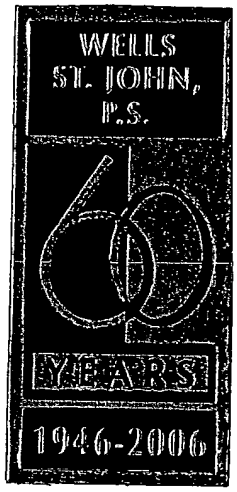

June 8, 2006

Via Federal Express and Certified Mail

Mr. J. Dennis Keller
1840 NW 10041 Ave
Pembrooke Pines, FL 33028

Re: U.S.A. Patent Application Serial No. 09/118,359
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Sincerely,

Robert C. Hyta

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